AMENDMENTS TO THE CLAIMS:

Please amend claims 41, 46-48, and 53 and 57-59 as shown below.

This listing of claims will replace all prior versions and listings of claims in the Application:

Claims 1-40 (cancelled)

Claim 41 (currently amended): A method of forming a circuit board, comprising the steps of:

a. providing a non-conducting substrate having a top surface and a bottom surface, said top surface comprising a first conductor layer and said bottom surface comprising a second conductor layer;

b. preheating the substrate from step a;

c. image printing a first resist pattern mask over a portion of said first conductor layer to form a plurality of first exposed areas;

d. image printing a second resist pattern mask over a portion of said second conductor layer to form a plurality of second exposed areas, wherein each of said plurality of first exposed areas is disposed above one of said plurality of second exposed areas;

e. plating said first and second exposed areas of said first and second conductor layers and removing said pattern masks and underlying conductor layers ~~first conductor from each of said plurality of first exposed areas~~ to form a plurality of first void areas on said top surface~~;~~

~~f. removing said second conductor from each of said plurality of second exposed areas to form~~ and a plurality of second void areas on said bottom surface;

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[[g]]f. forming a plurality of vias by connecting one of said plurality of first void areas with one of said plurality of second void areas;

g. seeding said plurality of vias with a conductive ink;

h. plating said plurality of vias to form said plurality of conductive pathways between said top surface and said bottom surface;

i. forming a first circuit pattern on said top surface by direct image printing ~~a conductive composition~~ an electrically-conductive ink onto said top surface using electro-photographic, ink jet, relief press or lithographic printing techniques; and

j. forming a second circuit pattern on said bottom surface by direct image printing ~~a conductive composition~~ an electrically-conductive ink onto said bottom surface using electro-photographic, ink jet, relief press or lithographic printing techniques.

Claim 42 (previously presented): The method of claim 41, further comprising the step of printing one or more circuit devices on said first circuit pattern and on said second circuit pattern.

Claim 43 (previously presented): The method of claim 42, wherein said circuit devices are selected from the group consisting of capacitors, inductors, resistors, transformers, and mixtures thereof.

Claim 44 (previously presented): The method of claim 43, wherein said first circuit pattern comprises a solderable component and a non-solder component, and further comprising the step of directly printing a solder mask on said non-solder component of said first circuit pattern and on said circuit devices printed on said first circuit pattern.

Claim 45 (previously presented): The method of claim 44, wherein said second circuit pattern comprises a solderable component and a non-solder component, and further comprising

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the step of directly printing a solder mask on said non-solder component of said second circuit pattern and on said circuit devices printed on said second circuit pattern.

Claim 46 (currently amended): ~~The method of claim 41, wherein step i further comprises:~~A method of forming a circuit board, comprising the steps of:

a. providing a non-conducting substrate having a top surface and a bottom surface, said top surface comprising a first conductor layer and said bottom surface comprising a second conductor layer;

b. preheating the substrate from step a;

c. image printing a first resist pattern mask over a portion of said first conductor layer to form a plurality of first exposed areas;

d. image printing a second resist pattern mask over a portion of said second conductor layer to form a plurality of second exposed areas, wherein each of said plurality of first exposed areas is disposed above one of said plurality of second exposed areas;

e. plating said first and second exposed areas of said first and second conductor layers and removing said pattern masks and underlying conductor layers to form a plurality of first void areas on said top surface and a plurality of second void areas on said bottom surface;

f. forming a plurality of vias by connecting one of said plurality of first void areas with one of said plurality of second void areas;

g. seeding said plurality of vias with a conductive ink;

h. plating said plurality of vias to form said plurality of conductive pathways between said top surface and said bottom surface;

i. direct image printing a resist pattern mask on said top surface to define said first circuit pattern;

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j. plating said top surface to increase the thickness of said first circuit pattern;

k. removing said resist pattern mask; [[and]]

l. removing any exposed first conductor layer; and

m. forming a second circuit pattern on said bottom surface by direct image printing a conductive composition onto said bottom surface using electro-photographic, ink jet, relief press or lithographic printing techniques.

Claim 47 (currently amended): ~~The method of claim 46, wherein step j further comprises:~~ A method of forming a circuit board, comprising the steps of:

a. providing a non-conducting substrate having a top surface and a bottom surface, said top surface comprising a first conductor layer and said bottom surface comprising a second conductor layer;

b. preheating the substrate from step a;

c. image printing a first resist pattern mask over a portion of said first conductor layer to form a plurality of first exposed areas;

d. image printing a second resist pattern mask over a portion of said second conductor layer to form a plurality of second exposed areas, wherein each of said plurality of first exposed areas is disposed above one of said plurality of second exposed areas;

e. plating said first and second exposed areas of said first and second conductor layers and removing said pattern masks and underlying conductor layers to form a plurality of first void areas on said top surface and a plurality of second void areas on said bottom surface;

f. forming a plurality of vias by connecting one of said plurality of first void areas with one of said plurality of second void areas;

g. seeding said plurality of vias with a conductive ink;

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h. plating said plurality of vias to form said plurality of conductive pathways between said top surface and said bottom surface;

i. forming a first circuit pattern on said top surface by direct image printing a conductive composition onto said top surface using electro-photographic, ink jet, relief press or lithographic printing techniques;

j. direct image printing a resist pattern mask on said bottom surface to define said second circuit pattern;

k. plating said bottom surface to increase the thickness of said second circuit pattern;

l. removing said resist pattern mask; and

m. removing any exposed second conductor layer.

Claim 48 (currently amended): A method of forming a multilayer circuit board, comprising the steps of:

a. providing a first substrate having a first top surface and a first bottom surface, whereas said first top surface comprises a first conductor layer and said first bottom surface comprises a second conductor layer;

b. preheating the substrate from step a;

c. image printing a first resist pattern mask over a portion of said first conductor layer to form a plurality of first exposed areas;

d. image printing a second resist pattern mask over a portion of said second conductor layer to form a plurality of second exposed areas, wherein each of said plurality of first exposed areas on said top surface is disposed above one of said plurality of second exposed areas on said bottom surface;

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e. plating said first and second exposed areas of said first and second conductor layers and removing said pattern masks and underlying conductor layers ~~first conductor from each of said first exposed areas~~ to form a plurality of first void areas on said top surface~~;~~

~~f. removing said second conductor from each of said plurality of second exposed areas to form~~ and a plurality of second void areas on said bottom surface;

[[g]]f. forming a plurality of vias by connecting one of said plurality of first void areas with one of said plurality of second void areas;

g. seeding said plurality of vias with a conductive ink;

h. plating said plurality of vias to form said plurality of conductive pathways between said first top surface and said first bottom surface;

i. forming a first circuit pattern on said first top surface by direct image printing of an electrically-conductive ink using electro-photographic, ink jet, relief press or lithographic printing techniques;

j. forming a second circuit pattern on said first bottom surface by direct image printing of an electrically-conductive ink using electro-photographic, ink jet, relief press or lithographic printing techniques;

k. supplying a second substrate having a second top surface and a second bottom surface;

l. forming a plurality of electrically conductive pathways between said second top surface and said second bottom surface;

m. forming a third circuit pattern on said second top surface by direct image printing of an electrically-conductive ink using electro-photographic, ink jet, relief press or lithographic printing techniques;

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n. forming a fourth circuit pattern on said second bottom surface by direct image printing of an electrically-conductive ink using electro-photographic, ink jet, relief press or lithographic printing techniques;

o. supplying a first insulating layer having a first side and a second side;

p. joining said first side of said first insulating layer to said first bottom surface, and joining said second side of said first insulating layer to said second top surface, such that said first insulating layer electrically insulates said second circuit pattern from said third circuit pattern; and

q. forming a plurality of electrically conductive pathways between said first circuit pattern, said second circuit pattern, said third circuit pattern, and said fourth circuit pattern.

Claim 49 (previously presented): The method of claim 48, further comprising the step of printing one or more circuit devices on said first circuit pattern, on said second circuit pattern, on said third circuit pattern, and on said fourth circuit pattern.

Claim 50 (previously presented): The method of claim 49, wherein said circuit devices are selected from the group consisting of capacitors, inductors, resistors, transformers, and mixtures thereof.

Claim 51 (previously presented): The method of claim 48, wherein step i further comprises:

image printing a resist mask on said first top surface to define said first circuit pattern;

plating said first top surface to increase the thickness of said first circuit pattern;

removing said mask; and

removing any exposed first conductor.

Claim 52 (previously presented): The method of claim 51, wherein step j further comprises:

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image printing a resist mask on said first bottom surface to define said second circuit pattern;

plating said bottom surface to increase the thickness of said second circuit pattern;

removing said mask; and

removing any exposed second conductor.

Claim 53 (currently amended): The method of claim 48, wherein said second top surface comprises a first conductor layer and said second bottom surface comprises a second conductor layer, and wherein step [[f]]e further comprises the steps of:

image printing a resist mask over a portion of said first conductor layer to form a plurality of first exposed areas;

image printing a resist mask over a portion of said second conductor layer to form a plurality of second exposed areas, wherein each of said plurality of first exposed areas on said top surface is disposed above one of said plurality of second exposed areas on said bottom surface;

removing said first conductor layer from each of said first exposed areas to form a plurality of first void areas on said top surface;

removing said second conductor layer from each of said plurality of second exposed areas to form a plurality of second void areas on said bottom surface;

forming a plurality of vias by connecting one of said plurality of first void areas with one of said plurality of second void areas;

plating said plurality of vias to form said plurality of conductive pathways between said second top surface and said second bottom surface.

Claim 54 (previously presented): The method of claim 53, wherein step m further comprises:

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direct image printing a resist mask on said second top surface to define said third circuit pattern;

plating said second top surface to increase the thickness of said third circuit pattern;

removing said mask; and

removing any exposed first conductor.

Claim 55 (previously presented): The method of claim 48, wherein step n further comprises:

direct image printing a resist mask on said second bottom surface to define said fourth circuit pattern;

plating said second bottom surface to increase the thickness of said fourth circuit pattern;

removing said mask; and

removing any exposed second conductor.

Claim 56 (previously presented): The method of claim 48, further comprising the steps of:

r. supplying a third substrate having a third top surface and a third bottom surface;

s. forming a plurality of electrically conductive pathways between said third top surface and said third bottom surface;

t. forming a fifth circuit pattern on said third top surface by direct image printing;

u. forming a sixth circuit pattern on said third bottom surface by direct image printing;

v. supplying a second insulating layer having a first side and a second side;

w. joining said first side of said second insulating layer to said second bottom surface, and joining said second side of said second insulating layer to said third top surface,

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such that said second insulating layer electrically insulates said fourth circuit pattern from said fifth circuit pattern; and

x. forming a plurality of electrically conductive pathways between said first circuit pattern, said second circuit pattern, said third circuit pattern, said fourth circuit pattern, said fifth circuit pattern, and said sixth circuit pattern.

Claim 57 (currently amended): The method of claim 56, wherein said third top surface comprises a [[first]]third conductor layer and said third bottom surface comprises a [[second]]fourth conductor layer, and wherein step [[m]]l further comprises the steps of:

direct image printing a resist pattern mask over a portion of said [[first]]third conductor layer to form a plurality of first exposed areas;

direct image printing a resist pattern mask over a portion of said [[second]]fourth conductor layer to form a plurality of second exposed areas, wherein each of said plurality of first exposed areas on said top surface is disposed above one of said plurality of second exposed areas on said bottom surface;

removing said [[first]]third conductor layer from each of said first exposed areas to form a plurality of first void areas on said top surface;

removing said [[second]]fourth conductor layer from each of said plurality of second exposed areas to form a plurality of second void areas on said bottom surface;

forming a plurality of vias by connecting one of said plurality of first void areas with one of said plurality of second void areas; and

plating said plurality of vias to form said plurality of conductive pathways between said first top surface and said first bottom surface.

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Claim 58 (currently amended): The method of claim 57, wherein step [[t]]s further comprises:

direct image printing a resist mask on said first top surface to define said fifth circuit pattern;

plating said first top surface to increase the thickness of said first circuit pattern;

removing said mask; and

removing any exposed first conductor.

Claim 59 (currently amended): The method of claim 58, wherein step [[u]]t further comprises:

direct image printing a resist mask on said first bottom surface to define said sixth circuit pattern;

plating said bottom surface to increase the thickness of said second circuit pattern;

removing said mask; and

removing any exposed second conductor.

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